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Influence of temperature and dimension in a 4H-SiC vertical power MOSFET

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Abstract

A study of the impact of dimension and temperature on a state of the art 4H-SiC power vertical DMOSFET has been carried out using drift-diffusion calculations in conjunction with electrical characterizations to extract physical parameters and doping profiles in a 6 μm channel length device. The model presented in this paper includes the effect of trapping in the channel/oxide interface. Using these parameters, the performance of corresponding lateral and vertical scaled devices are studied. Electrothermal simulations showing self-heating effects are also carried out. The results are qualitatively discussed with the help of an analytical physical model, which considers the interplay between the different device resistances. At low drain bias, the drain current is increased by 42.86% ($I_D = 5$ A at $V_G = 20$ V) when reducing the dimension vertically, whereas it is decreased by 28.57% ($I_D = 2.5$ A at $V_G = 20$ V) when reducing the dimension laterally. These effects are enhanced at high drain bias. In addition, the effect of dimension reduction for breakdown voltage, electric field and impact ionization is investigated. A substantial reduction in breakdown voltage was found when the vertical dimensions were decreased as compared to the lateral dimensions.

1. Introduction

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the most attractive semiconductor device for integrated circuit (ICs). Vertical double diffused MOSFETs (VDMOSFET) have the advantage of having a thick drift region to support the large current and high breakdown voltage for power applications. MOSFETs are used either as a switch or as an amplifier in the circuit [1]. For power applications, MOSFETs made of Silicon have some physical limitations such as low breakdown field and low thermal conductivity. However, Silicon Carbide (SiC) MOSFETs are highly recommended for their minimum cooling requirements and large density current capabilities (due mostly to a large breakdown field and relatively large thermal conductivity). SiC MOSFETs are promising candidates for future railway and aeronautical applications as they can deliver considerably large energy densities [2].

Nowadays, there is an increased attraction in improving low-voltage power FET technologies to be used in different applications like switched-mode power converters, automotive electronics, high-frequency lamp ballasts, medical electronics, smart-power ASICs, motor control, and aerospace electronics. The high input impedance is a crucial factor in power MOSFETs with an insulated gate, which enhances the control of the circuit design. These devices are certainly considered faster than devices that run in a bipolar mode [3].

In high-frequency power switching applications, such as high-density power supplies, there is a signal delay due to the parasitic resistive-capacitive elements and the effect of that delay in power devices is an order of magnitude larger in size than small-signal devices. The power devices need to exhibit high reliability when

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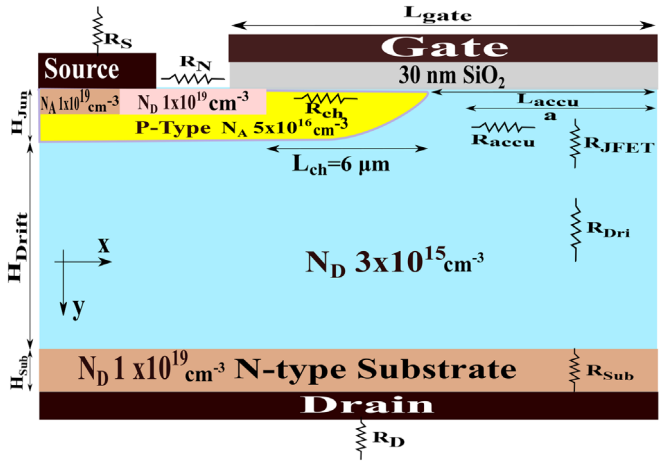


Figure 1. Structure of 4H-SiC vertical DMOSFET with parameters, doping concentration profile and resistances.

delivering power to large inductive loads. It is shown that an optimum die size exists for a given device technology which results in minimal conduction and switching power losses [4].

Vertical MOSFETs are more suitable for extreme scaling as vertical devices have more room between contacts and spacers than FinFETs and lateral stacked MOSFET architectures [5]. The scaling transistor technology gives an opportunity for a better amplification of low gate voltage devices in order to implement low switching pulses [6]. There is a huge interest in scaling the die size of SiC power devices to achieve high-current rated devices up to 150 A, which are relevant for the performance of high SiC power modules [7]. In general design rules for power MOSFET aim to reduce device dimensions but to keep larger current capabilities, high speed switching time and large blocking voltages. The vertical MOSFET architecture already partially decouples the blocking voltage, which is controlled by the size and doping of the epitaxial layer, from the current capability, which is controlled by the channel dimensions [8]. Scaling tries to reduce On-resistances and therefore the power dissipation but to keep large voltage blocking capabilities. Field guard rings are usually added to reduce or smooth high field regions in the external surfaces of the device as surface junctions exhibit substantially lower breakdown than the quasi-1D junction in planar structures. In order to fabricate a more compact converter with reduced thermal handling and material usage, a reduction in device dimensions is required. However, small dimensions usually tend to crowd the field resulting in a reduction of breakdown voltage. Compact power MOSFET designs are also needed for the integration of power modules into the CMOS IC technology. Furthermore, the commonly used Silicon dioxide (SiO2) dielectric should be substituted or combined with high-κ dielectrics in order to reduce leakage, dielectric breakdown, and improve electrostatic control when scaling [9].

The development of CMOS and power MOS devices (vertical and lateral DMOSFET) makes the integration of CMOS and power devices on the same SiC wafer possible, necessary for developing smart power IC's. When the complexity of smart power systems is increased, CMOS technologies employ some enhanced functions for full control and protection. Device dimensions scaling is one of these enhanced functions, and the main target is to increase the circuit speed and density. The scaling techniques used to develop the submicron CMOS technology in SiC power devices have become the core of smart power applications [10].

The increased temperature in a SiC n-channel layer leads to a noticeable reduction in the operating frequency, which is due to the decreased device conductivity. The results of these approaches would motivate the researchers to design and enhance future devices with the necessary optimizations such as scaling dimensions and gate oxide [11]. In addition, the continued downscaling of transistor dimensions calls for highly conductive electrodes (source and drain). Otherwise, the current through the device would be limited by the contacts [12]. The transconductance of the device improves and the threshold voltage decreases at high temperature as fewer electrons are trapped in the interface states, which results in a MOS channel resistance reduction [13].

In this paper, we study the behaviour of both lateral and vertical scaling of a state of the art 6 μm channel length power SiC vertical DMOSFET. The work starts by measuring the current/voltage characteristicand the breakdown voltage of a fabricated device. These characteristics are used to calibrate drift diffusion-based current-voltage characteristic. The simulated current-voltage characteristic agreed with the experimental ones for a broad range of biases and temperatures. From the calibration process, device dimensions, doping and trap concentration are extracted by using the corresponding material/device properties such as wide bandgap, impact ionization and mobility model [14]. By using the above parameters and considerations, the original



Figure 2. Measurement snapshot using Sony/Tektronix (371A) high power curve tracer.

Table 1. The parameters used in our simulation in the mobility model to obtain good agreement with the measured data.

⟨1100⟩	Values	Units	⟨0001⟩	Values	Units
μ_1	30	$cm^2/(V.s)$	μ_1	5	$cm^2/(V.s)$
μ_2	450	$cm^2/(V.s)$	μ_2	80	$cm^2/(V.s)$
a	−3	arbitrary	a	−3	arbitrary
b	−3	arbitrary	b	−3	arbitrary
c	0	arbitrary	c	0	arbitrary
d	0.5	arbitrary	d	0.5	arbitrary
NCR	13e17	cm^{-3}	NCR	13e17	cm^{-3}

device dimensions are scaled vertically and horizontally with and without scaling of the gate oxide, and the calculated current-voltage characteristics are analysed qualitatively using an analytical model. We have also simulated the breakdown voltage and electric field for the scaled devices.

This paper is organized as follows. Section 2 introduces the device structure and simulation methodology. Section 3 presents the scaling simulation results and discussions. Finally, the conclusion is presented in section 4.

2. Device structure, measurements and simulation methodology

In this section, the structure of a half-cell 4H-SiC vertical DMOSFET is presented followed by experimental measurements, a description of the simulation methodology and calibration results.

Firstly, figure 1 illustrates the simplified cross-section of the 4H-SiC DMOSFET.The MOS channel length is 6 μm. The gate oxide thickness is set to 30 nm and the device width is 10 cm [2, 15]. The donor concentration of n-epi region which has been used in the simulation is $N_D = 3 \times 10^{15} cm^{-3}$ [2, 15, 16]. In addition, figure 1 shows also the relevant resistances affecting the carrier transport and its related locations.

Secondly, the measurements were performed on Cree device model (C2M1000170D [17] using a Sony/Tektronix high power curve tracer (the industry leader in high power curve tracers and is used for testing a wide variety of power semiconductors. It performs DC parametric characterization of thyristors, SCRs and power MOSFETs). The measurement snapshot using Sony/Tektronix is shown in figure 2. Computer software utilised in the measurement is Interactive Characterization Software (ICS), ICS provides point and click measurements, intuitive matrix control, built-in database tools, and graphical analysis capabilities for a total system solution. It is designed to control semiconductor test equipment used for device characterization and other microelectronics measurements. The measurements were carried out at room temperature.

Thirdly, the simulations of the device mentioned are carried out using the TCAD Silvaco software [17]. The drift-diffusion (DD) equations are solved self-consistently with Poisson's equation in order to calculate the current-voltage characteristics. For the electrothermal simulation, the Fourier heat equation is additionally solved in order to calculate the local device temperature. Thermal resistances were introduced as a boundary condition in the drain contact. This thermal resistance is calibrated to produce a maximum internal temperature of 423 K according to the safe functioning of the device.

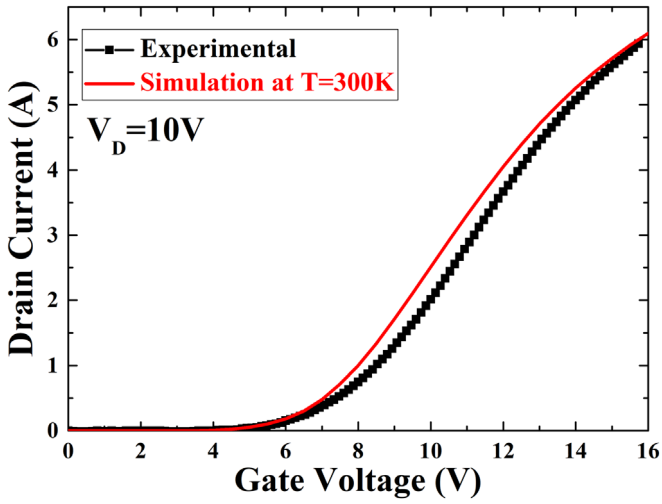


Figure 3. Transfer Characteristics at $V_D = 10$ V comparing between the experimental and simulation at $T = 300$ K.

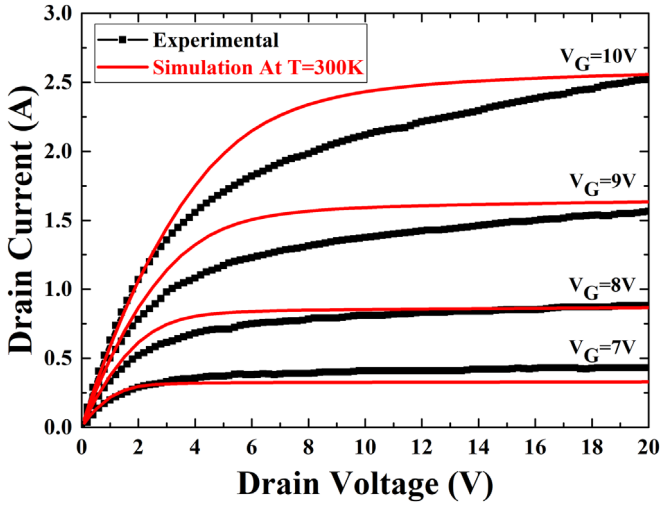


Figure 4. $I_D - V_D$ family curves comparing between the experimental and simulation at $T = 300$ K for $V_G = 7$ V to $V_G = 10$ V.

In our simulation, the acceptor interface traps have been used to model the bias-dependent charge trapping occurring in the interface oxide/semiconductor in the device channel [18]. Drift velocity variations at high field strength are modelled with an analytic mobility model based on Caughey-Thomas model [19–21]:

$$\mu_n(n, T_L) = \mu_1\left(\frac{T_L}{300}\right)^a + \frac{\mu_2\left(\frac{T_L}{300}\right)^b - \mu_1\left(\frac{T_L}{300}\right)^a}{1 + \left(\frac{T_L}{300}\right)^c\left(\frac{n}{NCR}\right)^d} \quad (1)$$

where n is the total doping concentration; T_L is the lattice temperature in Kelvin; μ 1 and μ 2 are the mobility of undoped samples; *NCR* is the doping concentration when the mobility has an average value between μ 1 and μ 2; d shows the rate of changing mobility from μ 1 to μ 2; a, b, c and d are temperature-dependent coefficients [19–21]. The parameters used in our simulation in the mobility model at $T_L = 300$ K are presented in table 1.

By comparing the measured current-voltage characteristics with the corresponding calculated characteristics, we have been able to estimate the dimensions, doping and physical parameters. An acceptor interface traps density of states of 2×10^{13} cm^{-2}/eV and a corresponding 0.1 eV band tail energy were found through the calibration process.

Finally, the calibrations of $I_D - V_D$ and $I_D - V_G$ of the device mentioned have been carried out based on the model mentioned above. Figure 3 shows the transfer characteristic ($I_D - V_G$) of the simulated device compared to the measurement results at a drain bias equal to 10 V. Note the good agreement with the experimental data. We need to draw attention to the fact that identical technological fabricated devices differ slightly in their

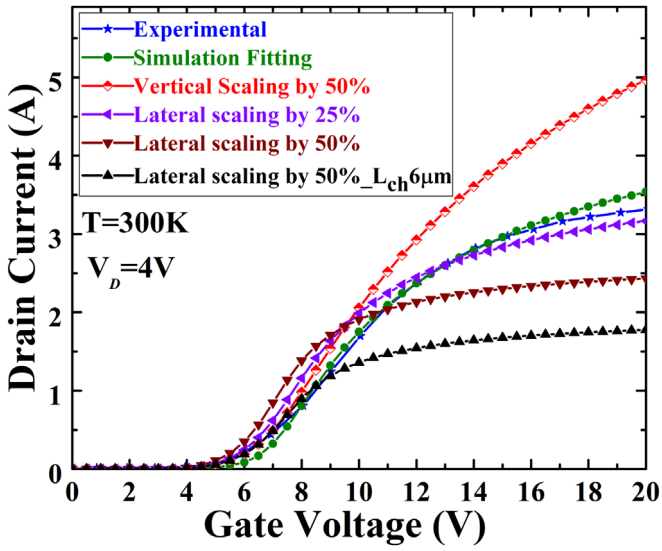


Figure 5. Transfer characteristics at $V_D = 4$ V comparing experimental, the simulation fitting, vertical and lateral scaling at room temperature.

characteristics. The corresponding drain currents versus drain bias at different gate bias are shown in figure 4. Note that the on-resistance and the on-current are similar in both the simulated and experimental curves.

3. Results and discussions

In this section, the $I_D - V_G$ characteristics of the scaled devices for low and high drain biases are presented, and both vertical and lateral scaling have been considered. In order to make our finding clear, a qualitative discussion using an analytical model based on the different device resistances is presented. In addition, we have carried out electrothermal simulations of the original and scaled devices by using a calibrated thermal resistance, which guarantees a maximum temperature of 423 K. Finally, calculation and analysis of the breakdown voltage of the scaled devices are illustrated.

The scaling up of the 4H-SiC power devices is beneficial to reduce the dislocation density from the current levels of low 10^4 cm^{-2} by at least an order of magnitude [22].

Figure 5 shows the transfer characteristics at low drain bias $V_D = 4$ V with vertical scaling by 50% and lateral scaling by 25/50%. In addition, lateral scaling by 50% but keeping the same channel length 6 μm is also presented. The figure illustrates that the drain current is increased by 42.86% ($I_D = 5$ A at $V_G = 20$ V) with vertical scaling, decreased by 8.57% ($I_D = 3.2$ A at $V_G = 20$ V) with the lateral scaling by 25%, decreased by 28.57% ($I_D = 2.5$ A at $V_G = 20$ V) with lateral scaling by 50% and decreased by 48.57% ($I_D = 1.8$ A at $V_G = 20$ V) with lateral scaling by 50% but keeping the same channel length 6 μm at high gate bias. This behaviour can be explained by using a simplified analytical model [15, 23] for the current-voltage characteristic. This model includes all major resistances contributing to the total on-resistance. These resistances are affected in different ways by the scaling procedures.

The equation for the drain current and the total on-resistance of the power vertical DMOSFET are shown below:

$$I_D = \begin{cases} 0 & for\ V_G < V_{TH} \\ R_{on}^{-1}\left(V_D - V_G + V_{TH} - \frac{1}{KR_{on}}\right) + \\ \sqrt{\left|\left(\frac{1}{KR_{on}^2} + \frac{V_G - V_{TH}}{R_{on}}\right)^2 - 2\frac{V_D}{KR_{on}^3}\right|} & \\ & for\ V_D \leqslant V_G - V_{TH} \\ \frac{K(V_G - V_{TH})^2(1 + \lambda V_D)}{2 + K(V_G - V_{TH})^2 \lambda R_{on}} & for\ V_D > V_G - V_{TH} \end{cases} \quad (2)$$

where K is a temperature-dependent transconductance coefficient and λ is the channel modulation coefficient. As mentioned before, the on-resistance comprises the algebraic sum of all the relevant resistances as depicted in figure 1. The notation for the different resistances are shown in the following equation [24]:

$$R_{on} = R_s + R_N + R_D + R_{ch} + R_{accu} + R_{JFET} + R_{Dri} + R_{Sub} \quad (3)$$

where R_S is a source resistance, R_N is a source N insulating resistance and R_D is a drain resistance. These resistances have a small effect on the total on-resistance and will not be considered in our approach [23, 24]. Our scaling analysis will focus on channel resistance R_{ch}, accumulation resistance R_{accu}, JFET region resistance R_{JFET}, drift region resistance R_{Dri} and substrate resistance R_{Sub}.

In a power vertical DMOSFET, the R_{on} is due to two channels connecting source to the drain. This produces a channel resistance given by [23, 24]:

$$R_{ch} = \frac{L_{ch}}{2W\mu_i C_{ox}(V_G - V_{TH})} \quad (4)$$

where L_{ch} is a channel length and W is a device width. The resistance contributed by the accumulation layer for the reason that the power vertical DMOSFET has two accumulation layers is [23, 24]:

$$R_{accu} = \frac{L_{accu}}{2\mu_A C_{ox}(V_G - V_{TH})} \quad (5)$$

where L_{accu} is the distance from the P-base region to the centre of the gate. The resistance contributed by the JFET region is [23, 24]:

$$R_{JFET} = \frac{\rho_{JFET} H_{jun}}{W(L_{gate} - 2H_{jun} - 2W_0)} \quad (6)$$

where ρ_{JFET} is the JFET region resistivity; H_{jun} is the P-Base junction depth; L_{gate} is the gate length and W_0 is the zero-bias depletion width in the JFET region. The resistance contributed by the drift region in the power vertical DMOSFET is [23, 24]:

$$R_{Dri} = \frac{\rho_{Dri}}{2W} ln\left[\frac{a + 2H_{drift}}{a}\right] \quad (7)$$

where ρ_{Dri} is the drift region resistivity; H_{drift} is the N-drift region depth and a is the width where the current flow in the drift region from the JFET region. The resistance contributed by N-substrate is [23, 24]:

$$R_{Sub} = \rho_{Sub} H_{sub} \quad (8)$$

where ρ_{Sub} is the substrate resistivity and H_{sub} is the substrate depth.

The vertical scaling mainly affects the JFET region resistance R_{JFET}, drift region resistance R_{Dri} and the substrate resistance R_{Sub}. These resistances are reduced with the vertical scaling by 42.86% at low drain bias and 18.88% at high drain bias. By using the expression of the resistances given before, we can estimate the percentage change of their value due to scaling. The JFET region resistance R_{JFET} is reduced by 62.5%, because the P-base junction depth H_{jun} is reduced by 50%. The drift region resistance R_{Dri} is reduced by 41.18%, because the H_{drift} is reduced by 50%. The substrate resistance R_{Sub} is reduced by 50%, because the substrate depth H_{sub} is reduced by 50% during the vertical scaling by 50%. This aforementioned decrease in resistance justifies the increase in current observed in the vertical scaled device. The results of a vertical scaling is suitable when self-heating effect is considered because the current is reduced at higher temperature. As the current is larger for vertical scaling, the device is less immune to a current reduction. Figure 5 presents that the on-current decreases when the device is scaled down laterally.

The lateral scaling mainly affects the channel resistance R_{ch}, the accumulation resistance R_{accu}, the JFET region resistance R_{JFET} and the drift region resistance R_{Dri}. R_{acc} and R_{ch} are mainly important at low gate bias while, the JFET and drift region resistance are mainly important at high gate bias. We have estimated the percentage change under lateral scaling of these resistances using the above formulas. The channel resistance is decreased by 50% when the channel length reduced by 50% during the lateral scaling by 50%. This justifies the relatively large current of the device with a 50% reduction of channel length relative to a similar device with the original channel length when comparing the two 50% laterally scaled devices. The channel length variation explains the change in the threshold voltage V_{th} between the curves shown in figure 5; the devices with the same channel length have the same threshold voltage V_{th}. However, the impact of channel resistance decreases with increasing gate bias. Consequently, by shrinking the channel by 25%, the channel resistance is decreased by 25%.

The accumulation resistance R_{accu} is decreased by 25% and 50% during the lateral scaling by 25% and 50%, respectively, because the distance from the P-base region to the center of the gate L_{accu} is reduced by 25% and 50%, respectively. However, the impact of the accumulation resistance decreases with increasing gate bias.

At high gate bias, JFET and drift region resistances are the main factor shaping the current behaviour. The JFET region resistance increased by 100% and 1900% during the lateral scaling by 25% and 50%, respectively, because the gate length is reduced by 25% and 50%. In addition, the drift region resistance is also increased by 17.65% and 47% during the lateral scaling by 25% and 50%, respectively. This is because the width where the

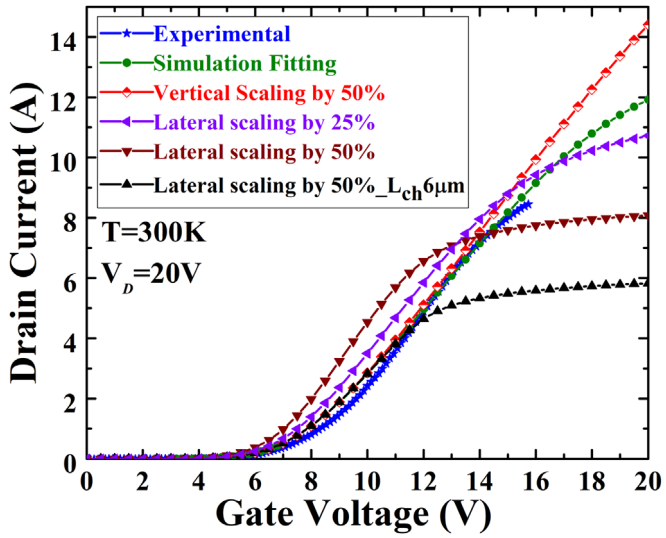


Figure 6. Transfer characteristics at $V_D = 20$ V comparing experimental, the simulation fitting, vertical and lateral scaling at room temperature.

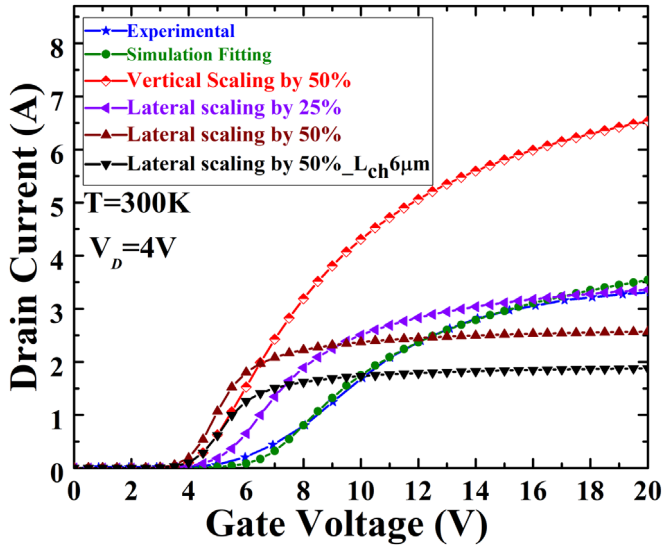


Figure 7. Transfer characteristics at $V_D = 4$ V comparing experimental, the simulation fitting, vertical and lateral scaling at room temperature with scaling gate oxide thickness the same proportion of scaling.

current flow in the drift region from JFET region is reduced by 25% and 50%, respectively. As a result, under lateral scaling at high gate bias, the R_{on} resistance increases and consequently the drain current is reduced.

Figure 6 shows the same characteristics shown in figure 5 but at high drain bias $V_D = 20$ V. The qualitative effect of the scaling at high drain bias is very similar to that at low drain bias. The figure shows that the drain current is increased by 18.83% ($I_D = 14.26$ A at $V_G = 20$ V) with vertical scaling, decreased by 10% ($I_D = 10.8$ A at $V_G = 20$ V) with the lateral scaling by 25%, decreased by 33.33% ($I_D = 8$ A at $V_G = 20$ V) with lateral scaling by 50%, and decreased by 51.67% ($I_D = 5.8$ A at $V_G = 20$ V) with lateral scaling by 50% but keeping the same channel length 6 μm at high gate bias. Figure 6 illustrates that the transfer characteristics at high drain bias $V_D = 20$ V provides a higher output resistance compared to low drain bias $V_D = 4$ V represented in figure 5, which is agreed with [25].

However, a scaling of the channel length requires other device parameters to be scaled suitably to avoid losses [23]. Oxide thickness is one of the parameters that need to be scaled down along with the channel length scaling [23] in order to keep the threshold voltage constant through scaling. In order to reduce the leakage current and avoid dielectric rupture, the oxide has to be substituted with a physically thicker oxide layer of higher dielectric constant (κ) [26].

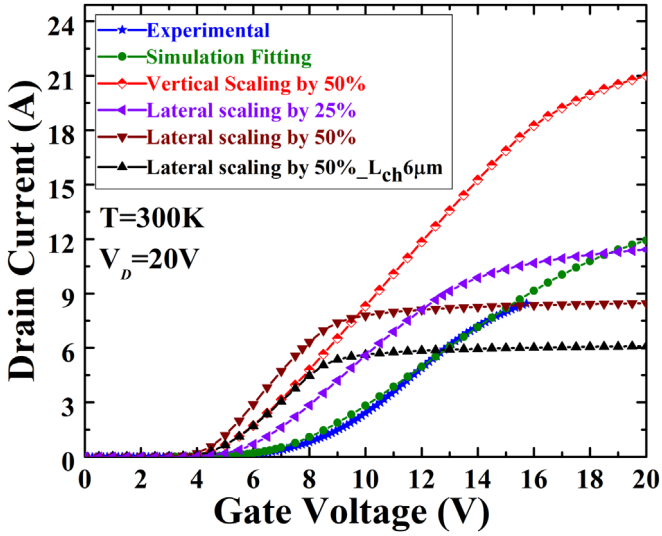


Figure 8. Transfer characteristics at $V_D = 20$ V comparing experimental, the simulation fitting, vertical and lateral scaling at room temperature with scaling gate oxide thickness the same proportion of scaling.

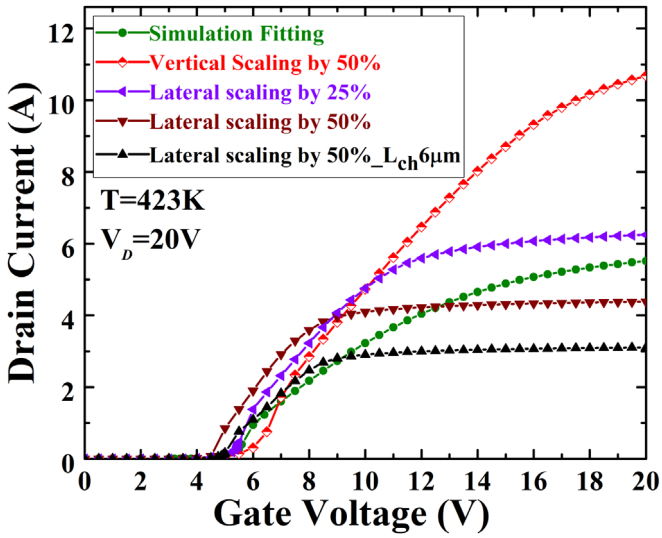


Figure 9. Transfer characteristics at $V_D = 20$ V comparing original simulated device, vertical and lateral scaled devices. The simulation used a thermal resistance which guarantees a maximum temperature of 423 K at $V_D = 20$ V, therefore self-heating is included.

Figure 7 shows the same characteristics of figure 5 but with the gate oxide thickness scale with the same proportion of scaling at low drain bias $V_D = 4$ V. Figure 8 shows the same characteristics of figure 7 but at high drain bias $V_D = 20$ V. it can be noticed in figures 7 and 8 that there is a shift in the threshold voltage and an increase in the drain current compared to figures 4 and 5. We have carried out electro-thermal simulations of the scaled device with/without scaling of the oxide at high drain V_D =20 V. It is found that there are significant effects on the transfer characteristics when the self-heating effect is applied. The specific thermal resistance is used to guarantee a safe maximum lattice temperature of 423 K.

Figures 9 and 10 show the transfer characteristics of scaled devices with unscaled and scaled oxide thickness respectively. The original device characteristic is shown for comparison. It should be noted that in figures 9 and 10, the temperature of the devices is different at each gate bias reaching a maximum at $V_G = 20$ V. Comparing the characteristics of the device in figure 7 (which shows the characteristic of room temperature devices) with those of figure 8, we see that the onset of the current is at a slightly early gate bias in figure 8. This is an effect of temperature dependence in the traps and is substantially explained in [2].

Figure 10 shows both reduction and saturation in the drain current as compared with the corresponding curves in figure 8. There is also a threshold voltage shift to the left when the oxide thickness is reduced as

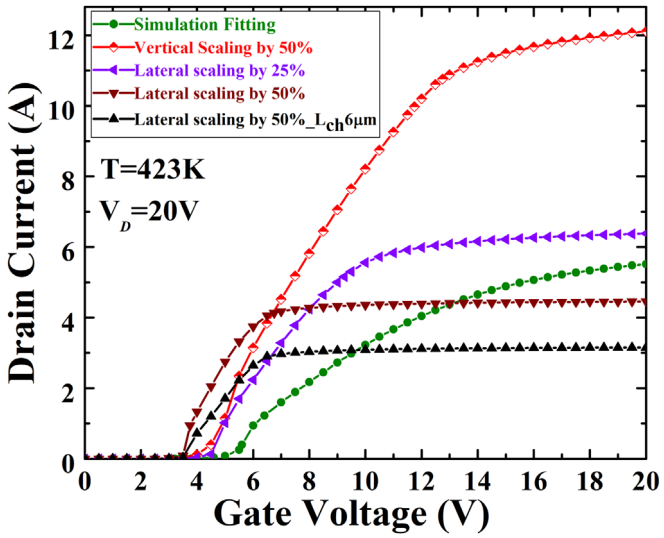


Figure 10. Transfer characteristics at $V_D = 20$ V of the experimental and simulated device. The simulation of vertically and laterally scaled device characteristics with the properly scaled oxide thickness is also shown. The simulation used a thermal resistance which guarantees a maximum temperature of 423 K at $V_D = 20$ V, therefore self-heating is included.

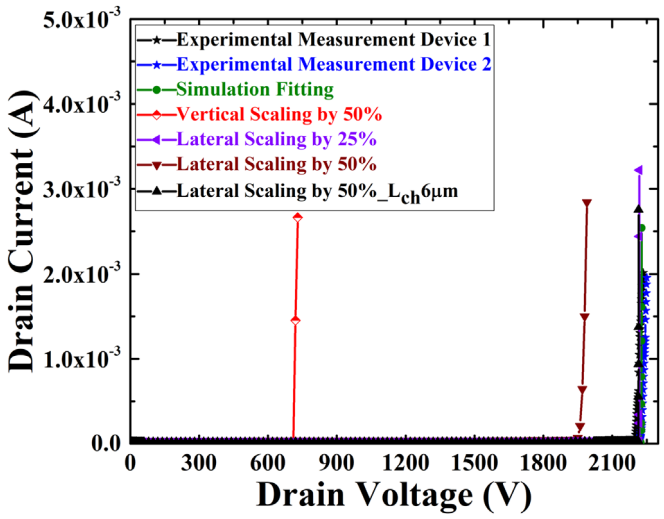


Figure 11. Breakdown voltage characteristics comparing (i) two experimental devices, (ii) the unscaled device, (iii) vertical scaled, (iv) two lateral scaled devices, one with channel length scaling and one without. Self-heating is included.

expected. It is shown that the threshold voltage is shifted to the left by 2 V, 0.5 V, 1 V and 1.5 V with the vertical scaling by 50%, horizontal scaling by 25%, horizontal scaling by 50%, and horizontal scaling by 50% but keeping the same channel length 6 μm, respectively. The purpose of scaling the gate oxide is to keep the threshold voltage down, as the input capacitance is increased with dimensional scaling [8].

The specific on-resistance of the original device at $V_G = 30$ V is equal to 29.3 mΩ.cm^2, which is very similar to the value provided by the manufacturer. The specific on-resistance of the vertical and lateral scaled down devices at $V_G = 30$ V are 19.8 mΩ.cm^2 and 24.1 mΩ.cm^2 respectively at room temperature. In the case of lateral scaling, the cell pitch area is considered to be half compared to the original device, while it is the same area for the vertical scaling case. The specific on-resistance at high temperature is investigated. The specific on-resistance of the vertical and lateral scaled devices at $V_G = 10$ V increases from 39.1 mΩ.cm^2 and 15.8 mΩ.cm^2 without including a self-heating to 53.4 mΩ.cm^2 and 31.6 mΩ.cm^2 respectively including self-heating to reach the maximum of $T = 423$ K by using an appropriate thermal resistance.

Finally, measurements and simulations of breakdown voltage were carried out for the scaled devices. We have measured the breakdown voltage for two identically fabricated devices. Small differences were noted due to slight differences in doping concentration.

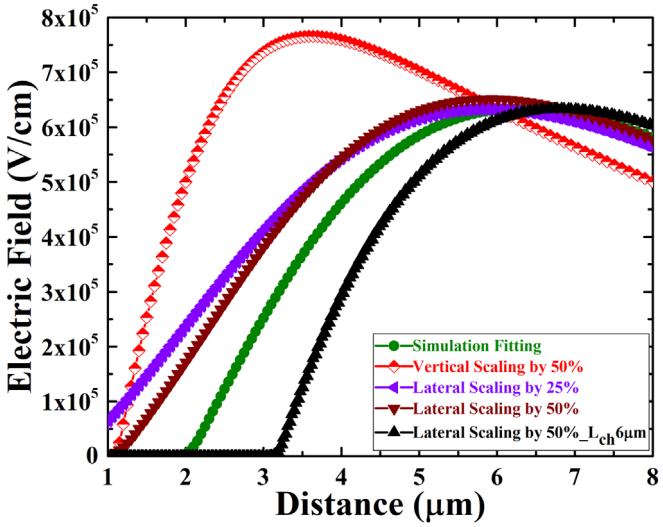


Figure 12. Electric field through the channel of the device at $V_D = 500$ V comparing the unscaled simulation device, vertical and lateral scaling with and without scaling channel length. Self-heating is included.

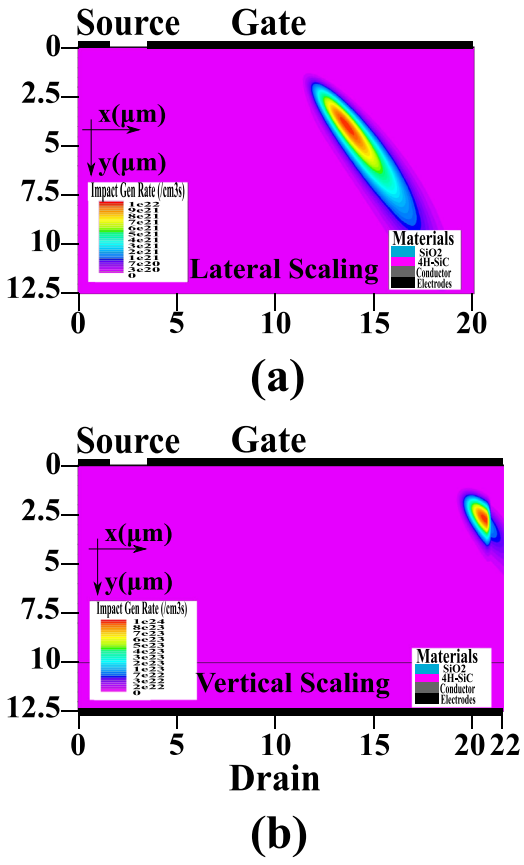


Figure 13. The device structure showing the impact generation rate at breakdown of (a) Lateral scaling for SiC VDMOSFET device by 50%. (b) Vertical scaling for SiC VDMOSFET device by 50%.

In order to minimize the possibility of damaging the test devices through high $\left(\frac{\delta I}{\delta V}\right)$ under avalanche conditions, a relatively high resistance (10 $K\Omega$) was placed in series with the device. This test configuration is in compliance with the latest industry standard test method [27]. The series resistance does not affect the voltage that device breakdown occurs, but reduces the $\left(\frac{\delta I}{\delta V}\right)$ in avalanche. This effect can be observed in the experimental results of figure 11, where the gradient of the $I - V$ characteristic post-breakdown is reduced.

Figure 11 shows a comparison between the experimental measurements, the simulation fitting and the scaled simulated devices. Vertical and horizontal scaling have been considered. Vertical scaling by 50% produces a large percentage reduction of 67.64% in the breakdown voltage ($B_V = 720$ V) however lateral scaling by 50% only produces a small percentage reduction of 12.36% ($B_V = 1950$V) compared to the original device breakdown ($B_V = 2225$V). The difference in breakdown voltage for vertical scaling can be attributed to the increase of electric field due to the decrease of the source-to-drain distance, however, there is also more crowding of the electric field as the dimensions are reduced. This is confirmed by the impact ionization rates (to be shown later in figure 13) which is very localized in the region of large curvature in the doping (under the gate region). In contrast, the reduction in the breakdown voltage with lateral scaling is substantially less as the vertical direction is not changed but still, the reduction of channel length increases the crowding of the field and consequently decrease the breakdown field. This is confirmed by the calculation of the breakdown voltage of the device with lateral scaling but keeping the channel length unchanged (see figure 11). In this case, the breakdown voltage was changed very little by just 0.45% ($B_V = 2215$V).

Figure 12 shows the electric field across the channel of devices at $V_D = 500$ V comparing between the simulation calibrated, vertical, lateral scaling and lateral scaling but keeping the same channel length at self-heating condition. This figure is a vertical cut-line through the region of maximum electric field for each of the devices. It shows that the device with higher electric field has lower breakdown voltage comparing to the other devices as expected.

Figures 13(a) and (b) illustrate the impact generation rate at the breakdown for both lateral and vertical scaling by 50% for SiC VDMOSFET device. Both figures have been plotted in the same scope at ($x = 20$ μm and $y = 12.5$ μm) in order to show the spread of the impact ionization due to crowding of the field. It is clear that the device with higher impact generation rate has lower breakdown voltage compared to the other devices and shows that the breakdown occurs very locally because the generation rate increases in the $p - n$ depletion region by two orders of magnitude with respect to the immediate surrounding.

4. Conclusion

The scaling process is a key factor for improving the switching speed of CMOS structures. This allows the fabrication of smaller electronic devices, which will fit new technologies and provide larger functionality. In this work, using advanced modelling simulation tools complemented with characterization, we have carried out the scaling of a fabricated device and explored its potential. Electro-thermal simulations were carried out and the results present a current degradation at high temperature. We are aware that with the current technology, vertical scaling is unprovable. However, the vertical scaling is performed in order to explore the impact on the current-voltage characteristic.

The reduction in breakdown voltage produced by lateral scaling can be avoided by keeping the channel length unchanged during scaling. This is because reducing the channel length increases the crowding of the field and consequently decreases the breakdown voltage. This has been demonstrated by carrying out breakdown voltage simulations of a lateral scaled device in which the channel length is left unchanged.

It was observed that vertical scaling provides a higher drain current, which is beneficial for high-temperature applications, but the breakdown voltage is reduced. The reduction of breakdown is substantial and should be mitigated by several techniques such as junction termination extension and guard rings, which reduce the high electric field near junction edges.

The oxide thickness was also scaled in the same proportions as the lateral scaling in order to keep the same electrostatic control as the original device. This will increase the possibility of oxide rupture. However, this could be mitigated by using higher dielectric constant (κ) and a small Silicon oxide layer close to SiC interface. In general, scaling will provide faster switching speeds as the device has good electrical control but higher current levels.

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